TEMIC

Siliconix

Si9707DY

PC Card (PCMCIA) Dual Interface Switch

Features

- Single SO-16 Package
- CMOS Logic Compatible Inputs
- Smart Switching
- Slow V_{CC} Ramp Times
- Extremely Low R_{ON}
- Supports Dual PC Card Slots
- Reverse Blocking Switches
- Low Power Consumption
- Safe Power-Up

Description

The Si9707DY offers an integrated solution for dual PC Card power interfaces that require only V_{CC} switching. This part is ideal for systems that operate at 5 V and provide V_{PP} from the main supply, or from a dedicated Flash RAM 12-V supply.

The Si9707DY operates off the 5-V supply with built-in level shifting. The V_{CC} outputs function independently and internal logic protects each slot against a control logic error

that would short 5 V to the 3.3-V supply. This protection logic also allows the Si9707DY to be configured for positive or negative control logic for compatibility with a variety of PC Card controllers. These control inputs are CMOS logic compatible and can be driven to 3.3 V or 5 V.

The PC Card Dual Interface Switch is available in a SO-16 narrow-body package and is rated over the industrial temperature range of −40 to 85°C.

Functional Block Diagram
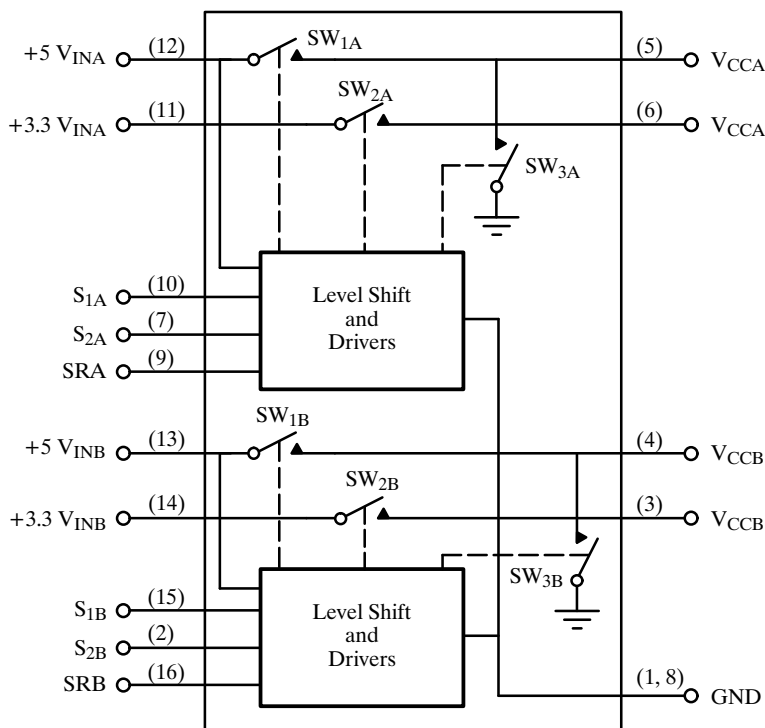
Absolute Maximum Ratings

Voltages Referenced to Ground
+5 V_{INA}, +5 V_{INB} . . . . 7 V
+3.3 V_{INA}, +3.3 V_{INB} . . . . 7 V
S_{1A} and S_{2A}, S_{1B}, S_{2B} (CMOS Inputs) . . . . 7 V
All Pins . . . . −0.5 V
I_{OUT} V_{CCA}[a], I_{OUT} V_{CCB}[b] . . . . 4 A
PD Max[c]: (T_A = 25°C) . . . . 1.65 W
(T_A = 85°C) . . . . 0.65 W

Junction Temperature . . . . 125°C
Thermal Ratings: $R_{\Theta JA}$[c] . . . . 60 °C/W
Notes
a. Pins 5, 6 connected together externally.
b. Pins 3, 4 connected together externally.
c. Mounted on 1-IN², FR4 PC Board.

Recommended Operating Conditions

+5 V_{INA}, +5 V_{INB} (must be present) . . . . 5 V ±10%
+3.3 V_{INA}, +3.3 V_{INB} . . . . 3.3 V ±10%
C_{SRA}, C_{SRB} . . . . 33 nF
I_{OUT} V_{CCA}[a], I_{OUT} V_{CCB}[b] . . . . 2 A

V_{CC} Load Capacitance . . . . 150 μF Max
Notes
a. Pins 5, 6 connected together externally.
b. Pins 3, 4 connected together externally.

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified C_{SR} = 33 nF, +5 V_{IN}= 5 V +3.3 V_{IN} = 3.3 V, Low ≤ 0.8 V, High ≥ 2.2 V		Limits −40 to 85°C			Unit
				Min[a]	Typ	Max[a]	
Switch SW$_{1A}$, SW$_{1B}$							
On-Resistance	R_{ON}	I = 500 mA, S_1 = High S_2 = Low	T_A = 25°C		58	70	mΩ
			T_A = 85°C		73	90	
Off Current (V_{CC})	I_{OFF}	+5 V_{IN} = 5.5 V, V_{CC} = 0 V S_1= S_2 = Low	T_A = 25°C			1	μA
			T_A = 85°C			10	
Rise Time	$t_{S1(on)}$	S_2 = Low, See Figure 1		0.2	1.7	5	ms
Fall Time	$t_{S1(off)}$			10	30	50	
Switch SW$_{2A}$, SW$_{2B}$							
On-Resistance	R_{ON}	I = 500 mA, S_2 = High S_1 = Low	T_A = 25°C		44	55	mΩ
			T_A = 85°C		55	70	
Off Current (+3.3 V_{IN})	I_{OFF}	+3.3 V_{IN} = 3.6 V, V_{CC} = 0 V S_1 = S_2= Low	T_A = 25°C			1	μA
			T_A = 85°C			10	
Rise Time	$t_{S2(on)}$	S_1 = Low, See Figure 1		0.1	0.9	5	ms
Fall Time	$t_{S2(off)}$			5	20	40	
Switch SW$_{3A}$, SW$_{3B}$							
On-Resistance	R_{ON}	I = 2 mA, S_1 = S_2 = Low	T_A = 25°C		140	400	Ω
			T_A = 85°C		200	500	
Power Supply							
+5 V_{IN} Current Input (on)	$I_{+5VIN(1)}$	S_1 = 0 V, S_2= 3 V			20	50	μA
	$I_{+5VIN(2)}$	S_1 = 3 V, S_2 = 0V			20	50	
+5 V_{IN} Current Input (off)	$I_{+5VIN(3)}$	S_1 = S_2= 0 V			< 1	10	
Switch Control Inputs S$_{1X}$, S$_{2X}$							
Input Voltage High	$V_{I(H)}$	+5 V_{INX} = 5.5 V		2.2	1.8		V
		+5 V_{INX} = 4.5 V		2.2	1.6		
Input Voltage Low	$V_{I(L)}$	+5 V_{INX} = 5.5 V			1.6	0.8	
		+5 V_{INX} = 4.5 V			1.4	0.8	
Input Current High	$I_{I(H)}$	S_{1X}, S_{2X} = 5 V				1.0	μA
Input Current Low	$I_{I(L)}$	S_{1X}, S_{2X} = GND		−1.0			

Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
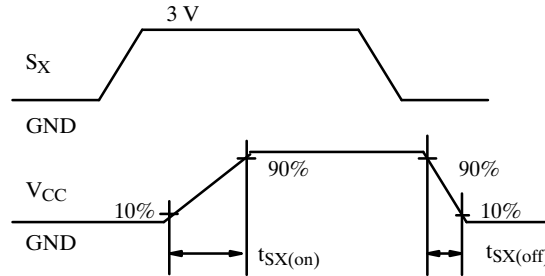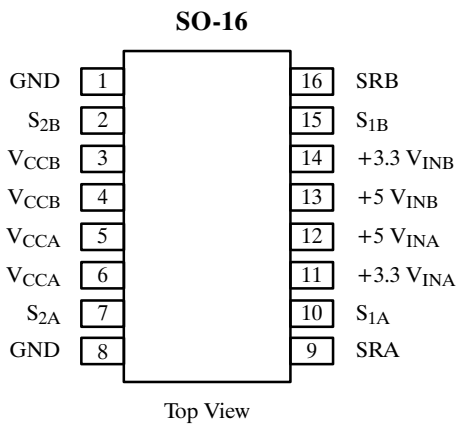
Timing Waveforms

Figure 1. Switch Ramp Time

Pin Configuration and Description

SO-16

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GND   [1]        [16]  SRB
S2B   [2]        [15]  S1B
VCCB  [3]        [14]  +3.3 VINB
VCCB  [4]        [13]  +5 VINB
VCCA  [5]        [12]  +5 VINA
VCCA  [6]        [11]  +3.3 VINA
S2A   [7]        [10]  S1A
GND   [8]        [9]   SRA
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Top View

Function	Pin Number	Description
S_{1A}	10	Control input for selecting +5 V_{INA} to V_{CCA}.
S_{1B}	15	Control input for selecting +5 V_{INB} to V_{CCB}.
S_{2A}	7	Control input for selecting +3.3 V_{INA} to V_{CCA}.
S_{2B}	2	Control input for selecting +3.3 V_{INB} to V_{CCB}.
GND	1, 8	Ground connection.
V_{CCA}	5, 6	Supply voltage to slot.
V_{CCB}	3, 4	Supply voltage to slot.
+3.3 V_{INA}	11	+3.3-V supply.
+3.3 V_{INB}	14	+3.3-V supply.
+5 V_{INA}	12	+5-V supply.
+5 V_{INB}	13	+5-V supply.
SRA	9	Slew rate control pin.
SRB	16	Slew rate control pin.

Truth Table

S_1X	S_2X	Switch 1X	Switch 2X	Switch 3X
0	0	Off	Off	On
0	1	Off	On	Off
1	0	On	Off	Off
1	1	Off	Off	On

Notes
a.   Switch 1 and 2 are delayed until after V_{CC} is valid.
b.   Shaded lines are error conditions for PC Card applications.
c.   The smart switching of the Si9707 avoids potential host damage by defaulting to off during error conditions.

Typical Characteristics (25°C Unless Otherwise Noted)

On-Resistance vs. Load Current

R_{ON} − On-Resistance (Ω)

Switch 1

Switch 2

I_D − Load Current (A)

On-Resistance vs. Junction Temperature

R_{ON} − On-Resistance (Ω)

$I_D = 1\,A$
$T_J = T_A$

Switch 1

Switch 2

T_J − Junction Temperature (°C)

Rise Time vs. SR Capacitor Value

$t_{SX(on)}$ − Rise Time (ms)

$C_{load} = 0\,pF$

Switch 1

Switch 2

Open

C_{SR} − Capacitor Value (nF)

Fall Time vs. SR Capacitor Value

$t_{SX(off)}$ − Fall Time (ms)

$C_{load} = 0\,pF$

Switch 1

Switch 2

Open

C_{SR} − Capacitor Value (nF)

Rise Time vs. Load Capacitance

$t_{SX(on)}$ − Rise Time (ms)

$C_{SR} = 33\,nF$

Switch 1

Switch 2

C_{load} − Load Capacitance (μF)

Fall Time vs. Load Capacitance

$t_{SX(off)}$ − Fall Time (ms)

$C_{SR} = 33\,nF$

Switch 1

Switch 2

C_{load} − Load Capacitance (μF)